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10/663,128	09/16/2003	Ken Gary Pomaranski	200308565-1	4003

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EXAMINER	
KIM, DANIEL Y	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,128	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed January 26, 2006 in response to the PTO Office Action mailed November 3, 2005. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, no claims have been canceled, amended or added. Claims 1-44 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 5-16 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545) and Shidla et al (US PGPub No. 20050050276).

For claim 1, Long discloses a system, comprising:

a memory mapping logic configured to provide access to memory locations (a virtual-physical memory mapping device for mapping one or more virtual memory addresses requested by the co-processor into corresponding physical addresses, col. 1, lines 35-38), where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location (col. 1, lines 35-38).

Despite these teachings, Long fails to disclose the remaining claim limitations.

Shidla, however, discloses a memory quality assurance logic (a memory controller includes a cache, par. 0014), where the memory quality assurance logic is configured to:

control copying contents between a first memory location and a second memory location (information from a portion of the memory is copied into the cache, par. 0014);

reconfigure the memory mapping logic so that memory accessing operations intended for the first memory location are directed to the second memory location (the memory controller directs accesses to the portion of the memory to the information stored in the cache, par. 0014); and

initiate memory testing of the first memory location (a test module causes tests to be performed on the portion of the memory, par. 0014).

Long and Shidla are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a memory quality assurance logic because it would be desirable to be able to detect errors in areas of a main memory of a computer system before the errors cause failures to occur during operation of the system (par. 0005), as taught by Shidla.

For claim 3, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Long further discloses the memory mapping logic includes one or more address translation tables (the virtual-physical memory mapping device further includes a multiple-entry translation lookaside buffer for caching virtual-to-physical address mappings, col. 1, lines 43-45).

For claim 5, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Long further discloses the memory quality assurance logic is configured to selectively logically remove the first memory location from a first set of memory by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location (the virtual-physical memory mapping device may include devices for comparing, replacing, singly invalidating and multiply invalidating one or more entries of the translation lookaside buffer, col. 1, lines 47-51).

For claim 6, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Long further discloses the memory quality assurance logic is configured to selectively logically replace the first memory location with the

second memory location by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location (the translation lookaside buffer is adapted to replace entries therein, col. 1, lines 45-46; the virtual-physical memory mapping device may include devices for comparing, replacing, singly invalidating and multiply invalidating one or more entries of the translation lookaside buffer, col. 1, lines 47-51).

Claim 7 is rejected using the same rationale as for the rejection of claim 6 above.

For claim 8, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Shidla further discloses the memory quality assurance logic is configured to initiate memory testing of the first memory location by sending one or more signals to a memory testing logic (after the contents of a memory portion are copied into the cache, the memory controller may provide an indication to the operating system that the portion is ready for testing, par. 0026).

For claim 9, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Long further discloses the memory quality assurance logic is configured to initiate memory testing of the first memory location by sending one or more signals to an onboard memory testing logic, where the onboard memory testing logic is physically connected to the first memory location (par. 0026; fig. 1, items 122, 129).

For claim 10, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Shidla further discloses the memory quality assurance logic selects the second memory location (the test engine selects a portion for testing

and causes a command to be provided to control logic and cache control to indicate that portion is to be tested, par. 0034).

For claim 11, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Shidla further discloses the memory quality assurance logic includes one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data (test engine detects errors in a memory portion during testing, and in response to detecting an error, the failing address or addresses in the portion may be logged, par. 0037).

For claim 12, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Shidla further discloses the memory quality assurance logic being operable connected to the one or more data stores (fig. 1, items 122, 129).

Claim 13 is rejected using the same rationale as for the rejection of claim 12 above.

Claim 14 is rejected using the same rationale as for the rejection of claim 12 above.

Claim 15 is rejected using the same rationale as for the rejection of claim 12 above.

Claim 16 is rejected using the same rationale as for the rejection of claim 10 above.

For claim 29, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Long further discloses:

a processor (a co-processor adapted for using virtual memory with a host processor device, col. 1, lines 30-31);

a memory operably connected to the processor, where the processor can access the memory (a memory coupled to the host processing device to implement the virtual memory, col. 1, lines 31-32);

For claim 30, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Long further discloses the system is embedded in a computer (fig.1 illustrates the operation of a co-processor within a host computer environment, col. 3, lines 16-17; fig. 1).

For claim 31, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 29 above. Long further discloses the system is embedded in an image forming device (a number of co-processors could be utilized to speed up various operations such as the production of graphical images for display or printing out, col. 1, lines 22-24).

Claim 32 is rejected using the same rationale as for the rejections of claims 11 and 29 above.

Claim 33 is rejected using the same rationale as for the rejections of claims 12 and 29 above.

For claim 34, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. Long further discloses a memory location selection logic configured to select the first memory location and the second memory location (interrogating a virtual memory table and mapping one or more virtual memory

addresses requested by the co-processor into corresponding physical addresses in the memory of the host processing device, col. 1, lines 61-64).

6. Claims 17-19 and 21-25, 28, 35-38 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545), Shidla et al (US PGPub No. 20050050276) and Leung et al (US PGPub No. 20050044467).

For claim 17, the combined teachings of Long and Shidla disclose the invention as per rejections of claims 1 and 6 above. These teachings fail to disclose the limitations of claim 17.

Leung, however, helps disclose initiating memory testing of the first memory location without an operating system interaction (a memory system with transparent error correction circuitry, abstract; from the outside of the memory, the ECC storage and logic are completely transparent, par. 0016).

Long, Shidla and Leung are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to make memory testing transparent to an operating system because this allows for error-correction in an embedded environment (par. 0008), as taught by Leung.

For claim 18, the combined teachings of Long, Shidla and Leung disclose the invention as per rejection of claim 17 above. Shidla further discloses access to the contents of the first memory location as copied to the second memory location can continue concurrently with the memory testing (during the tests, the memory controller

directs accesses to the portion of the memory to the information stored in the cache, par. 0014).

Claim 19 is rejected using the same rationale as for the rejection of claim 17 above.

Claim 21 is rejected using the same rationale as for the rejection of claim 17 above.

Claim 22 is rejected using the same rationale as for the rejections of claims 5 and 17 above.

Claim 23 is rejected using the same rationale as for the rejections of claims 5 and 17 above.

Claim 24 is rejected using the same rationale as for the rejection of claims 11 and 17 above.

Claim 25 is rejected using the same rationale as for the rejections of claims 11 and 17 above.

Claim 28 is rejected using the same rationale as for the rejection of claim 21 above.

Claim 35 is rejected using the same rationale as for the rejection of claim 17 above.

Claim 36 is rejected using the same rationale as for the rejection of claims 21 and 35 above.

Claim 37 is rejected using the same rationales as for the rejection of claims 5 and 17 above.

Claim 38 is rejected using the same rationale as for the rejections of claims 17 and 29 above.

Claim 41 is rejected using the same rationale as for the rejections of claims 5 and 38 above. Shidla further discloses after the tests are complete, the information is copied from the cache back into the portion of the memory (par. 0014).

Claim 42 is rejected using the same rationale as for the rejection of claims 5 and 38 above.

Claim 43 is rejected using the same rationale as for the rejection of claims 5 and 38 above.

7. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545), Shidla et al (US PGPub No. 20050050276), Leung et al (US PGPub No. 20050044467) and Nakamura (US Patent No. 6,523,135).

For claim 26, the combined teachings of Long, Shidla and Leung disclose the invention as per rejection of claim 17 above. These teachings fail to disclose the limitations of claim 26.

Nakamura, however, helps disclose testing the first memory location includes two or more test methods (a built-in self-test circuit for a memory including a test mode controller, abstract; including its own microprocessor for generating test patterns such as column bars, checker board, marching, shifted diagonal test and other test patterns, col. 1, lines 15-18).

Long, Shidla, Leung and Nakamura are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include such tests because this would help to test substantially all the functions or any desired functions of a memory (col. 2, lines 24-25), as taught by Nakamura.

Claim 27 is rejected using the same rationale as for the rejection of claim 26 above.

8. Claims 2, 40 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545), Shidla et al (US PGPub No. 20050050276) and Idleman et al (US Patent No. 5,274,645).

For claim 2, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. These teachings fail to disclose the limitations of claim 2.

Idleman, however, discloses error correction circuitry can be connected to all memories through a series of multiplexer circuits called crossbar switches (col. 4, lines 13-16).

Long, Shidla and Idleman are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include crossbar switches because they can be used to decouple failed memories from the system (col. 4, lines 16-17), as taught by Idleman.

Claim 40 is rejected using the same rationale as for the rejections of claims 2 and 38 above.

Claim 44 is rejected using the same rationale as for the rejections of claims 2 and 38 above. Idleman further discloses error correction or redundancy data and error detection data is generated "on the fly" (col. 3, lines 62-64).

9. Claims 4, 20 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545), Shidla et al (US PGPub No. 20050050276) and Chauvel et al (US PGPub No. 20040024970).

For claim 4, the combined teachings of Long and Shidla disclose the invention as per rejection of claim 1 above. These teachings fail to disclose the limitations of claim 4.

Chauvel helps disclose the memory quality assurance logic is configured to select the first memory location by one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method (a method for managing memory in which replacement algorithms may include, random replacement, round robin replacement, and least recently used replacement, par. 0018).

Long, Shidla and Chauvel are analogous art in that they are of the same field of endeavor, that is, a method for memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include such methods for

managing memories because this may reduce the number of memory accesses and overall power consumption (abstract), as taught by Chauvel.

Claim 20 is rejected using the same rationale as for the rejection of claims 4 and 17 above.

Claim 39 is rejected using the same rationale as for the rejection of claims 4 and 38 above.

Contact Information

10. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

4-17-06

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PRIMARY EXAMINER